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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/675,816 | 09/28/2000 | Gregory A. Overkamp | 10559/270001/P9277-ADI | 9784 |

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FISH & RICHARDSON, PC
4350 LA JOLLA VILLAGE DRIVE
SUITE 500
SAN DIEGO, CA 92122

| EXAMINER |
|---|
| HARKNESS, CHARLES A |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 5 |

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/675,816 | OVERKAMP, GREBORY A. ET. AL. | |
| | Examin r | Art Unit | |
| | Charles A Harkness | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Papers Submitted*

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Revised Declaration as received on 01/16/01; and Change of Address as received on 12/16/02

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiell et al, U.S. Patent Number 6,138,232 (herein referred to as Shiell).

Referring to claims 1 and 14 Shiell has taught a method of handling instructions within a processor comprising:

Decoding at least a portion of an instruction coded in a first code (Shiell column 4 line 59-column 5 line 3; predecode unit 0 decodes the x86 instructions, and determines the size and position; figure 1 reference number 128);

Re-encoding the at least a portion of the instruction to a second code if necessary (Shiell column 4 line 59-column 5 line 3; predecode unit 1 recodes the multi-byte instructions into a fixed length format; figure 1 reference number 132); and

Forwarding the re-encoded instruction to a destination (Shiell column 4 line 59-column 5 line 27; the decode unit and the scheduler send the instruction onto the execution units, they work together for the final step of determining where the instruction will go; figure 1 reference numbers 134 and 136).

Referring to claims 2 and 15 Shiell has taught further comprising:

The decoder determining the destination of the instruction (Shiell column 4 line 59-column 5 line 27; the decode unit and the scheduler send the instruction onto the execution units, they work together for the final step of determining where the instruction will go; figure 1 reference numbers 134 and 136).

Referring to claim 3 Shiell has taught further comprising sending at least a portion of the coded instruction to a functional unit (Shiell column 4 line 59-column 5 line 27; the coded

instruction is sent to the predecode 0 unit from the fetch unit, and the predecode unit is a functional unit of the system; figure 1 reference numbers 126-136).

Referring to claim 4 Shiell has taught further comprising sending at least a portion of the decoded instruction to a functional unit (Shiell column 4 line 59-column 5 line 27; the decoded instruction is sent to the predecode 1 unit from the predecode 1 unit, and the predecode unit is a functional unit of the system; figure 1 reference numbers 126-136).

Referring to claim 5 Shiell has taught further comprising determining a portion of the coded instruction to decode (Shiell column 4 line 59-column 5 line 3; predecode 0 unit determines the length and position of the x86 instructions to be decoded; figure 1 reference numbers 128).

Referring to claim 6 Shiell has taught further comprising forwarding the re-encoded instruction to a functional unit (Shiell column 4 line 59-column 5 line 27; the recoded instruction is sent to the decode and scheduler from the predecode 1 unit, and the decode unit is a functional unit of the system; figure 1 reference numbers 126-136).

Referring to claim 7 Shiell has taught further comprising handling instructions in a digital signal processor (Shiell abstract figure 1, columns 1 and 2; the processor described would use digital signals to send data and controls throughout the microprocessor, thus making it a digital signal processor).

Referring to claim 8 Shiell has taught a method of processing instruction within a processor comprising:

Receiving an instruction which is coded in a first code (Shiell column 4 line 25-column 5 line 27; the instruction is fetched from cache; figure 1 reference numbers 126-136);

Determining at least a destination location for the instruction (Shiell column 4 line 59-column 5 line 27; sending the instruction from the fetch unit to the predecode 1 unit; figure 1 reference numbers 126-136);

Forwarding any portion of the coded instruction having a destination location of a first location (Shiell column 4 line 59-column 5 line 27; sending the instruction from the fetch unit to the predecode 1 unit; figure 1 reference numbers 126-136);

Decoding any remaining portion of the instruction (Shiell column 4 line 59-column 5 line 27; predecode unit 0 decodes the x86 instructions, and determines the size and position; figure 1 reference numbers 126-136);

Forwarding any portion of the decoded instruction having a destination location to a second location (Shiell column 4 line 59-column 5 line 27; the decoded instruction is sent to the predecode 1 unit from the predecode 1 unit, and the predecode unit is a functional unit of the system; figure 1 reference numbers 126-136);

Re-encoding any remaining portion of the instruction to a second code if necessary (Shiell column 4 line 59-column 5 line 3; predecode unit 1 recodes the multi-byte instructions into a fixed length format; figure 1 reference number 132); and

Forwarding the re-encoded instruction to a third location (Shiell column 4 line 59-column 5 line 27; the decode unit and the scheduler send the instruction onto the execution units, they work together for the final step of determining where the instruction will go; figure 1 reference numbers 134 and 136).

Referring to claim 9 Shiell has taught wherein said forwarding steps comprise forwarding the instruction to the first, second, and third locations which comprise functional units (Shiell

column 4 line 59-column 5 line 27; the recoded instruction is sent to the decode and scheduler from the predecode 1 unit, and the decode unit is a functional unit of the system, the predecode units are also functional units; figure 1 reference numbers 126-136).

Referring to claim 10 Shiell has taught further comprising forwarding any portion of the decoded instruction having a destination location of a second location to a data address generator (Shiell column 4 line 59-column 5 line 27; the decoded instruction will go to the load/store unit, 140, if it is a load or store instruction; figure 1 reference numbers 126-136, 140).

Referring to claim 11 Shiell has taught further comprising forwarding the re-encoded instruction to a system pipe (Shiell column 4 line 59-column 5 line 27; the recoded instruction is sent to the next functional unit in the pipelined system; figure 1 reference numbers 126-136).

Referring to claim 12 Shiell has taught further comprising processing instructions with a digital signal processor (Shiell abstract figure 1, columns 1 and 2; the processor described would use digital signals to send data and controls throughout the microprocessor, thus making it a digital signal processor).

Referring to claim 13 Shiell has taught further comprising decoding and re-encoding with a decoder (Shiell column 4 line 59-column 5 line 27; figure 1 reference numbers 126-136).

Referring to claim 16 Shiell has taught wherein the decoder forwards control signals to other portions of the processor (Shiell column 4 line 59-column 5 line 27; shown in figure 1, the decoder forwards control and data signals to the next functional unit in the pipeline; figure 1 reference numbers 126-136).

Referring to claim 17 Shiell has taught wherein the control signals may be in the first code or the second code (Shiell column 4 line 59-column 5 line 27; from the predecode they will

be in the first code, from the second predecode they will be in the second code; figure 1 reference numbers 126-136).

Referring to claim 18 Shiell has taught wherein the processor is a digital signal processor (Shiell abstract figure 1, columns 1 and 2; the processor described would use digital signals to send data and controls throughout the microprocessor, thus making it a digital signal processor).

***Conclusion***

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Black et al, U.S. Patent Number 5,619,408, has taught a method and system for recoding noneffective instructions within a data processing system.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

September 6, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100